

1497 Rec'd PCT/PTO 13 JAN 2006

PATENT
450101-04870.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Koichiro KISHIMA et al. #5
Serial No.: 10/540,720
International Application No.: PCT/JP04/16188
International Filing Date: October 25, 2004
For: METHOD FOR MANUFACTURING
SEMICONDUCTOR SUBSTRATE AND
SEMICONDUCTOR SUBSTRATE
Confirmation No.: 2419

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New York, NY 10151

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Box PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 9, 2006.

Thomas F. Presson, Reg. No. 41,442

Name of Applicant, Assignee or Registered Representative


Signature

January 9, 2006

Date of Signature

COMMUNICATION

Mail Stop Box PCT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed herewith is a copy of the "Notification of Missing Requirements" (form PCT/DO/EO/905) dated December 23, 2005 on the above application, a Declaration duly signed

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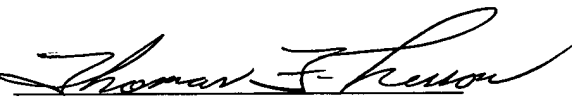
by the inventor and a check in the amount of the required \$130.00 surcharge. By separate cover, we are filing the Assignment and the \$40.00 fee for recording same.

Please charge any additional fees incurred or credit any overpayment to Deposit Account No. 50-0320.

In view of the foregoing, it is believed that the identified application is now complete. Early examination of the application on its merits is solicited.

Respectfully submitted,

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